Listing of the Claims

The following listing of claims will replace all prior versions and listings of the claims in the application:

1. (Currently Amended) A method of resetting a jam latch comprising:

combining a respective data signal from each of a plurality of data in signal lines in an activation device, the activation device having an output coupled to ~~activate~~ a first reset device;

activating a second reset device with a control signal; ~~and~~

applying a reset voltage to a storage cell including coupling the ~~rest~~ reset voltage across the activated first reset device and across the activated second ~~rest~~ reset device;

outputting a voltage from a voltage source controller, the voltage source controller includes a control input coupled to the output of the activation device, the voltage source controller further includes a voltage input coupled to a voltage source; and

applying the voltage to the output of the storage cell.

2. (Currently Amended) The method of claim 1, wherein combining a respective data signal from each of a plurality of data in signal lines in an activation device, the activation device having an output coupled to ~~activate~~ a first reset device includes:

coupling the respective data in signal from each of the plurality of data in signal lines to an activation device; and

outputting an activation signal, from the activation device to the first reset device, when a level of the respective data in signal from each of the plurality of data in signal lines is substantially equal.

3. (Original) The method of claim 1, wherein the control signal includes a clock signal.

4. (Original) The method of claim 1, wherein the control signal is inverted.

5. (Currently Amended) The method of claim 1, further comprising disconnecting ~~a voltage~~ the voltage source from the storage cell.

6. (Original) The method of claim 5, wherein the voltage source is disconnected from the storage cell substantially simultaneously with activating the first reset device.

7. (Canceled)

8. (Previously Presented) The method of claim 1, wherein the plurality of data in signal lines includes two or more data in signal lines.

9. (Currently Amended) A jam latch reset circuit comprising:

an activation device having respective inputs coupled to each one of a plurality of data in signal lines;

a first reset device having a first control input coupled to an output of the activation device, the first reset device having a reset voltage source coupled to an input of the first reset device;

a second reset device having a second control input coupled a control signal, the second reset device being coupled in series with the first reset device; ~~and~~

a storage cell coupled to an output of the second reset device, the storage cell having an input and an output, the second reset device having an output coupled to the storage cell output, and the storage cell input coupled to an input transistor; and

a voltage source coupled to the output of the storage cell through a voltage source controller, the voltage source controller includes a control input coupled to the output of the activation device.

10. (Previously Presented) The circuit of claim 9, wherein the output of the storage cell is coupled to the output of the second reset device.

11. (Original) The circuit of claim 9, wherein the control signal is a timing signal.

12. (Original) The circuit of claim 9, wherein the activation device is a logic device.

13. (Original) The circuit of claim 9, wherein the activation device is a nand gate.

14. (Canceled)

15. (Canceled)

16. (Currently Amended) The circuit of claim 9~~claim 14~~, wherein each of the voltage source controller, the first reset device, and the second reset device include transistors.

17. (Previously Presented) The circuit of claim 9, wherein the plurality of data in signal lines includes two or more data in signal lines.

18. (Previously Presented) The circuit of claim 9, wherein the storage cell includes a cross coupled inverter pair, the storage cell input being on an opposite side of the cross coupled inverter pair from the storage cell output.

19. (Currently Amended) A method of capturing data in a jam latch circuit comprising:

receiving a respective data in signal on at least one of a plurality of data in signal lines;

charging a storage cell on storage cell input;

outputting a data signal from a storage cell output;

combining the respective data in signal from each of the plurality of data in signal lines and the data signal from the storage cell output;

outputting a jam latch output data signal; and

resetting a jam latch circuit including:

combining the respective data in signal from each of the plurality of data in signal lines in an activation device, the activation device having an output coupled to ~~activate~~ a first reset device;

activating a second reset device with a control signal; ~~and~~

applying a reset voltage to the storage cell including coupling the reset voltage across the activated first reset device and across the activated second reset device;

outputting a voltage from a voltage source controller, the voltage source controller includes a control input coupled to the output of the activation device, the voltage source controller further includes a voltage input coupled to a voltage source; and

applying the voltage to the output of the storage cell.

20. (Currently Amended) The method of claim 19, wherein combining the respective data signal from each of the plurality of data in signal lines in an activation device, the activation device having an output coupled to ~~activate~~ the first reset device includes:

coupling the respective data in signal from each of the plurality of data in signal lines to an activation device; and

outputting an activation signal, from the activation device to the first reset device, when a level of the respective data in signal from each of the plurality of data in signal lines is substantially equal.